

Abstract of the Disclosure

A fuse option for a dynamic random access memory (DRAM) is provided to selectively slow row address signals when redundant rows of memory cells have been selected for use. The fuse option is blown when a redundant row is used to replace a defective row as identified during manufacture of a DRAM. The fuse is coupled to delay circuitry which has a known delay. When the fuse is blown after detecting a defective row, the delay circuitry is coupled in series with selected portions of a row address strobe (RAS) chain of circuitry used to propagate row address selection signals to the proper rows. This provides extra time needed for row address compare and override circuitry, which is not in series with the delay circuitry.

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